CLAIMS

What is claimed is:

1. A memory structure comprising a plurality of row conductors intersecting a plurality of column conductors at a plurality of intersections, each said intersection including an electrically linear resistive element in series with a voltage breakdown element.

2. The memory structure as defined in Claim 1, wherein the electrically linear resistive element is selected from the group consisting of intrinsic silicon, lightly doped microcrystalline silicon, lightly doped amorphous silicon, refractory metal silicide nitride, and tungsten silicide nitride.

3. The memory structure as defined in Claim 1, wherein the electrically linear resistive element has an electrical characteristic that, for linear changes in voltage, has a linear change in current.

4. The memory structure as defined in Claim 1, wherein the plurality of rows and the plurality of column form a memory device selected from the group consisting of a write-once-read-many (WORM) memory device and a one time programmable memory device.

5. The memory structure as defined in Claim 4, wherein the memory device is in a digital film for use in a digital camera.

6. The memory structure as defined in Claim 4, wherein the memory device is in a memory card.

7. The memory structure as defined in Claim 1, wherein the voltage breakdown element comprises an antifuse.

8. The memory structure as defined in Claim 7, wherein the antifuse is unpatterned.

9. The memory structure as defined in Claim 1, wherein the electrically linear resistive element comprises intrinsic silicon and the voltage breakdown element comprises an antifuse having a dielectric with a thickness not greater than about 200 Angstroms.

10. The memory structure as defined in Claim 1, wherein:
each of the row and column conductors are patterned; and
the electrically linear resistive element is patterned; and
the voltage breakdown element is not patterned.

11. An apparatus including the memory structure as defined in Claim 1, wherein the apparatus is selected from the group consisting of a digital camera, a hand held scanner, a desk top scanner, a fax machine, a copier, a multifunction peripheral (MFP), and a digital network copier.

12. A memory structure comprising a primary plurality of memory elements each including a row conductor connected to a column conductor by an electrically linear resistive element in series with a voltage breakdown element.

13. The memory structure as defined in Claim 12, wherein the electrically linear resistive element is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride, and tungsten silicide nitride.

14. The memory structure as defined in Claim 12, wherein the electrically linear resistive element is selected from the group consisting of an electrical device having an electrical characteristic that, for linear changes in voltage, has a linear change in current.

15. The memory structure as defined in Claim 12, wherein the voltage breakdown element is an antifuse that includes a dielectric having a thickness not greater than about 200 Angstroms.

16. The memory structure as defined in Claim 12, wherein:

each said electrically linear resistive element is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

each said voltage breakdown element comprises an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

17. The memory structure as defined in Claim 12, wherein:

each said row conductor and each said column conductor comprises patterned aluminum or an alloy thereof;

the electrically linear resistive element comprises patterned intrinsic silicon; and

the voltage breakdown element comprises unpatterned aluminum oxide having a thickness not greater than about 200 Angstroms.

18. The memory structure as defined in Claim 12, further comprising:

a secondary electrical insulator upon and over the said primary plurality of memory elements;

a secondary plurality of said memory elements stacked over said primary plurality of memory elements and on the secondary electrical insulator;

a third electrical insulator upon and under the said primary plurality of memory elements; and

a third plurality of said memory elements stacked under said primary plurality of memory elements and on the third electrical insulator.

19. The memory structure as defined in Claim 12, further comprising:

a secondary plurality of memory elements each including one said column conductor of said primary plurality of memory element connected to a row conductor by an electrically linear resistive element in series with a voltage breakdown element;

a third plurality of memory elements each including one said row conductor of said primary plurality of memory element connected to a column conductor by an electrically linear resistive element in series with a voltage breakdown element.

20. The memory structure as defined in Claim 19, wherein for each of the second and third plurality of memory elements:

each said row and column conductor comprises patterned aluminum or an alloy thereof;

the electrically linear resistive element comprises patterned intrinsic silicon; and

the voltage breakdown element comprises unpatterned aluminum oxide having a thickness not greater than about 200 Angstroms.

21. An apparatus including the memory structure as defined in Claim 12, wherein the apparatus is selected from the group consisting of a computing device, a multifunction peripheral, a cellular telephone, a personal digital assistant, a facsimile machine, a desk top scanner, a high volume copier, a music playing device, a video playing device, and a portable or fixed electronic apparatus utilizing the memory structure for permanent or removable memory media.

22. A memory structure comprising a plurality of adjacent pairs of row conductors each having there between:

an electrically linear resistive material;

a voltage breakdown material; and

a column conductor.

23. The memory structure as defined in Claim 22, wherein each said pair of adjacent row conductors also has an electrical insulator there between.

24. The memory structure as defined in Claim 22, wherein the voltage breakdown material is a layer of unpatterned material between each said pair of adjacent row conductors.

25. The memory structure as defined in Claim 22, wherein:

the electrically linear resistive material is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the voltage breakdown material comprises an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

26. A memory structure comprising a plurality of adjacent pairs of patterned row conductors each having there between a voltage breakdown element sandwiched between a column conductor and an electrically linear resistive element in series with the voltage breakdown element.

27. The memory structure as defined in Claim 26, wherein each said pair of adjacent row conductors also has an electrical insulator there between.

28. The memory structure as defined in Claim 26, wherein:

a layer of unpatterned material is between each said pair of adjacent row conductors; and

the layer of unpatterned material is the voltage breakdown element.

29. The memory structure as defined in Claim 26, wherein:

the electrically linear resistive element is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the voltage breakdown element comprises an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

30. A memory structure comprising a plurality of means for storing data; wherein:

each said means for storing data includes a row conductor connected to a column conductor by:

means for providing electrically linear resistance; and

means for programming the means for storing data;

the means for providing electrically linear resistance is in series with the means for programming the means for storing data.

31. The memory structure as defined in Claim 30, wherein the means for programming the memory element is a voltage breakdown element.

32. The memory structure as defined in Claim 31, wherein:

the voltage breakdown element comprises an antifuse;

each of the row and column conductors is patterned;

the electrically linear resistive element is patterned; and

the voltage breakdown element is not patterned.

33. A memory storage device comprising:

a substrate; and

a plurality of memory elements on the substrate, wherein:

each said memory element is included in a memory apparatus selected from the group consisting of a WORM memory device and a one time programmable memory device and includes:

a row conductor connected to a column conductor by an electrically linear resistive element in series with a voltage breakdown element.

34. The memory storage device as defined in Claim 33, wherein the memory apparatus is in a data storage device selected from the group consisting of a memory card and a digital film for use in a digital camera.

35. A method comprising forming a plurality of row conductors to intersect with a plurality of column conductors at a plurality of intersections, each said intersection including an electrically linear resistive element in series with a voltage breakdown element.

36. The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

depositing a first layer of column material;

patterning the first layer of column material to form the plurality of column conductors;

forming a voltage breakdown material on the plurality of column conductors;

forming an electrically linear resistive material upon the voltage breakdown material;

patterning the electrically linear resistive material;

depositing a layer of row material upon the patterned electrically linear resistive material;

patterning the layer of row material to form the plurality of row conductors.

37. The method as defined in Claim 36, further comprising forming an electrical insulator upon the voltage breakdown material and the patterned electrically linear resistive material.

38. The method as defined in Claim 36, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the electrical insulator and the voltage breakdown material.

39. The method as defined in Claim 36, wherein:

the electrically linear resistive material is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the voltage breakdown material comprises an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

40. The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

forming a first electrical insulator;

depositing a first layer of column material over the first electrical insulator;

patterning the first layer of column material to form the plurality of column conductors;

forming a first voltage breakdown material on the plurality of column conductors;

forming a first electrically linear resistive material upon the first voltage breakdown material;

depositing a first layer of row material upon the first electrically linear resistive material; and

patterning the first layer of row material to form a first plurality of row conductors;

forming a second electrical insulator upon the first plurality of row conductors;

depositing a second layer of column material over the second electrical insulator;

patterning the second layer of column material to form a second plurality of column conductors;

forming a second voltage breakdown material on the second plurality of column conductors;

forming a second electrically linear resistive material upon the second voltage breakdown material;

depositing a second layer of row material upon the second electrically linear resistive material; and

patterning the second layer of row material to form a second plurality of row conductors.

41. The method as defined in Claim 40, wherein:

at least one of the first and second electrical insulators is unpatterned;

at least one of the first and second voltage breakdown materials is unpatterned; and

at least one of the first and second electrically linear resistive materials is patterned.

42. The method as defined in Claim 40, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the first and second electrical insulator and the first and second voltage breakdown materials.

43. The method as defined in Claim 40, wherein:

the first and second electrically linear resistive materials are selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the first and second voltage breakdown materials comprise an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

44. The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

depositing a first layer of row material;

patterning the first layer of row material to form the plurality of row conductors;

forming a first voltage breakdown material on the plurality of row conductors;

forming a first electrically linear resistive material upon the first voltage breakdown material;

depositing a layer of column material upon the first electrically linear resistive material;

patterning the layer of column material to form the plurality of column conductors;

forming a second voltage breakdown material on the plurality of column conductors;

forming a second electrically linear resistive material upon the second voltage breakdown material;

depositing a second layer of row material upon the second electrically linear resistive material; and

patterning the second layer of row material to form another plurality of said row conductors.

45. The method as defined in Claim 44, wherein:

the first voltage breakdown material, upon which the first electrically linear resistive material is formed, is unpatterned;

the first electrically linear resistive material, upon which the first layer of column material is deposited, is patterned;

the second voltage breakdown material, upon which the second electrically linear resistive material is formed, is unpatterned;

the second electrically linear resistive material, upon which the second layer of row material is deposited, is patterned.

46. The method as defined in Claim 44, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the first voltage breakdown material and the second voltage breakdown material.

47. The method as defined in Claim 44, wherein:

the first and second electrically linear resistive materials are selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the first and second voltage breakdown materials comprise an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

48. A memory structure made by the method of Claim 35.

49. The memory structure as defined in Claim 48, further comprising a primary of memory elements, wherein each one said row conductor connected to one said

column conductor by one said electrically linear resistive element in series with one said voltage breakdown element.

50. The memory structure as defined in Claim 49, wherein each said memory element is in a memory device selected from the group consisting of a WORM memory device and a one time programmable memory device.

51. The memory structure as defined in Claim 49, wherein the memory device is included in a memory apparatus that is selected from the group consisting of a digital film and a memory card.